Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

Claim 1 (canceled)

Claim 2 (canceled)

Claim 3 (canceled)

Claim 4 (canceled)

Claim 5 (canceled)

Claim 6 (canceled)

Claim 7 (canceled)

Claim 8 (canceled)

Claim 9 (canceled)

Claim 10 (canceled)

Claim 11 (canceled)

Claim 12 (canceled)

Claim 13 (canceled)

Claim 14 (canceled)

Claim 15 (canceled)

Claim 16 (canceled)

Claim 17 (canceled)

Claim 18 (canceled)

Claim 19 (canceled)

Claim 20 (canceled)

Claim 21 (canceled)

Claim 22 (canceled)

Claim 23 (canceled)

Claim 24 (new): A semiconductor substrate material for producing a semiconductor substrate, the semiconductor substrate material comprising:

a multitude of hollow microspheres, each one of the multitude of hollow microspheres having an inner layer and an outer layer, the inner layer comprising a first material, the outer layer comprising a second material, and the first material and the second material differing from one another.

Claim 25 (new): The semiconductor substrate material in accordance with claim 24,

wherein the multitude of hollow microspheres comprises a multitude of gas filled ceramic microspheres.

Claim 26 (new): The semiconductor substrate material in accordance with claim 25, wherein at least one of the multitude of gas filled ceramic microspheres is sintered together with another one of the multitude of gas filled ceramic microspheres.

Claim 27 (new): The semiconductor substrate material in accordance with claim 25, wherein a hardened matrix contains the multitude of gas filled ceramic microspheres.

Claim 28 (new): The semiconductor substrate material in accordance with claim 25, wherein a glaze is disposed on a top surface of the semiconductor substrate.

Claim 29 (new): The semiconductor substrate material in accordance with claim 25, wherein the second material of the outer layer comprises a glass material, the inner layer of each of the gas filled ceramic microspheres has a first given melting point, the outer layer of the glass material has a second given melting point, and the first given melting point is higher than the second given melting point.

Claim 30 (new): The semiconductor substrate material in accordance with claim 29, wherein the outer layer of glass material of one of the multitude of gas filled ceramic microspheres is sintered to the outer layer of glass material of another one of the multitude of gas filled ceramic microspheres.

Claim 31 (new): The semiconductor substrate material in accordance with claim 24, wherein the multitude of hollow microspheres comprises a multitude of gas filled glass microspheres.

Claim 32 (new): The semiconductor substrate material in accordance with claim 31, wherein at least one of the multitude of gas filled glass microspheres is sintered together with another one of the multitude of gas filled glass microspheres.

Claim 33 (new): The semiconductor substrate material in accordance with claim 31, wherein a hardened matrix contains the gas filled glass microspheres.

Claim 34 (new): The semiconductor substrate material in accordance with claim 31, wherein a glaze is disposed on a top surface of the semiconductor substrate.

Claim 35 (new): The semiconductor substrate material in accordance with claim 31, wherein the second material of the outer layer comprises a glass material, the inner layer of each of the gas filled glass microspheres has a first given melting point, the outer layer of the glass material has a second given melting point, and the first given melting point is higher than the second given melting point.

Claim 36 (new): The semiconductor substrate material in accordance with claim 35, wherein the glass material of the outer layer of one of the multitude of gas filled glass microspheres is sintered to the glass material of the outer layer of another one of the multitude of gas filled glass microspheres.

Claim 37 (new): The semiconductor substrate material in accordance with claim 24, wherein at least one of the multitude of hollow microspheres is sintered together with another one of the multitude of hollow microspheres.

Claim 38 (new): The semiconductor substrate material in accordance with claim 24, wherein a hardened matrix contains the multitude of hollow microspheres.

Claim 39 (new): The semiconductor substrate material in accordance with claim 38, wherein the hardened matrix containing the multitude of hollow microspheres comprises glass particles, a binder material, and a viscosity modifier.

Claim 40 (new): The semiconductor substrate material in accordance with claim 39, wherein the binder material comprises at least one chosen from the group consisting

of ethyl cellulose, an acrylic, a polyvinyl alcohol, an organic polymer, and a borophosphate glass.

Claim 41 (new): The semiconductor substrate material in accordance with claim 39, wherein the at least one viscosity modifier comprises at least one chosen from the group consisting of a surfactant, an organic thickener, a magnesium silicates thickening agent, and a filler material.

Claim 42 (new): The semiconductor substrate material in accordance with claim 24, wherein a glaze is disposed on a top surface of the semiconductor substrate.

Claim 43 (new): The semiconductor substrate material in accordance with claim 24, wherein the first material of the inner layer has a first given melting point, the second material of the outer layer has a second given melting point, and the first given melting point is at higher than the second given melting point.

Claim 44 (new): The semiconductor substrate material in accordance with claim 43, wherein the outer layer of one of the multitude of hollow microspheres is sintered to the outer layer of another one of the multitude of hollow microspheres.

Claim 45 (new): The semiconductor substrate material in accordance with claim 24, wherein the semiconductor substrate forms a semiconductor wafer.

Claim 46 (new): The semiconductor substrate material in accordance with claim 24, wherein the semiconductor substrate forms an integrated circuit die.